

Getting Started with the Virtex-7 FPGA VC707 Evaluation Kit

UG848 (v1.1) March 1, 2013



Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/31/12	1.0	Initial Xilinx release.
03/01/13	1.1	Add Vivado Design Suite to VC707 Evaluation Kit Contents . Removed references to USB flash drive throughout Chapter 1, Getting Started with the Virtex-7 FPGA VC707 Evaluation Kit . Updated Step 1 and removed note in Extract the AMS Design Files, page 17 .

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Getting Started with the Virtex-7 FPGA VC707 Evaluation Kit

Introduction

This document describes how to use the materials provided in the VC707 Evaluation Kit to set up the VC707 board and a host computer to run three reference designs, which test and demonstrate some of the key features of the XC7VX485T FPGA and the VC707 board:

- Built-in self test (BIST)
- Integrated bit error rate test (IBERT)
- Analog mixed signal (AMS) card demonstration

Three additional reference designs that are compatible with the VC707 board are also summarized in this guide.

- Multiboot
- Memory interface generator (MIG)
- Integrated endpoint block for PCI EXPRESS®, and LogiCORE™ IP Ethernet

VC707 Evaluation Kit Contents

The VC707 Evaluation Kit includes:

- VC707 board with the Virtex®-7 XC7VX485T FPGA
- ISE® Design Suite: Logic Edition (full seat, device-locked to the XC7VX485T FPGA)
- Vivado™ Design Suite Installation DVD
- Printed entitlement voucher: provides entitlement of the Vivado Design Suite Logic Edition device-locked to the XC7VX485T FPGA. Follow the printed instructions on the voucher to redeem your software entitlement.
- AMS101 evaluation card
- USB cable, standard-A plug to mini-B plug
- USB cable, standard-A plug to micro-B plug
- HDMI™ cable, type-A plug to type-A plug
- Power Supply: 100 VAC–240 VAC input, 12 VDC 5.0A output
- Power cords to support three main plug types

- Getting Started Guide

Host Computer Requirements

The example designs described in this document require an Intel processor based computer running Windows 7 or Windows XP operating system. The computer must have two USB ports and an Ethernet interface.

Note: The Windows 7 operating system is used in the setup instructions and examples.

Preliminary Setup

Complete the tasks in this section before running the reference designs.

Install ISE Software

Install the latest version of the Xilinx ISE Design Suite on the host computer.

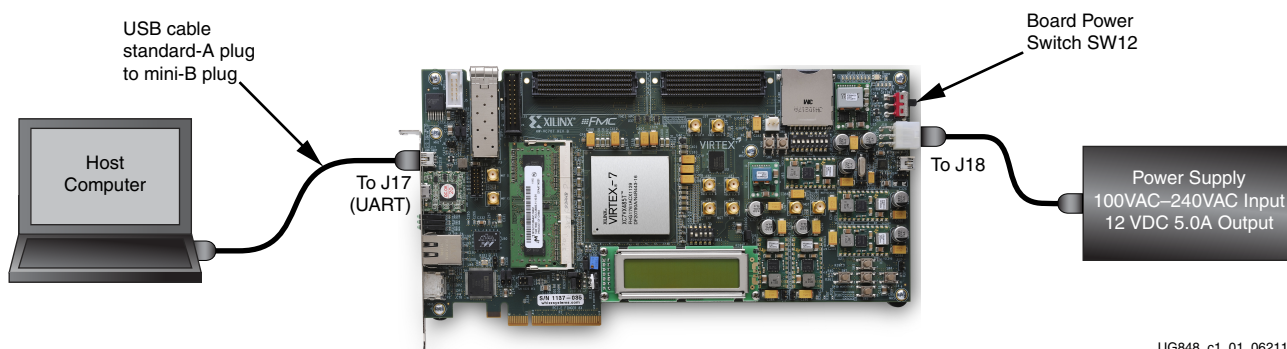
Install the USB UART Drivers

Download and install the Silicon Laboratories CP210x VCP drivers on the host computer. The drivers are available for download at no cost from www.silabs.com/Support/Documents/Software/CP210x_VCP_Win_XP_S2K3_Vista_7.exe.

Configure the Host Computer COM Port

The BIST design uses a terminal program to communicate between the host computer and the VC707 board. To configure the host computer COM port for this purpose:

1. Connect the VC707 board to the host computer and power supply as shown in [Figure 1-1](#).

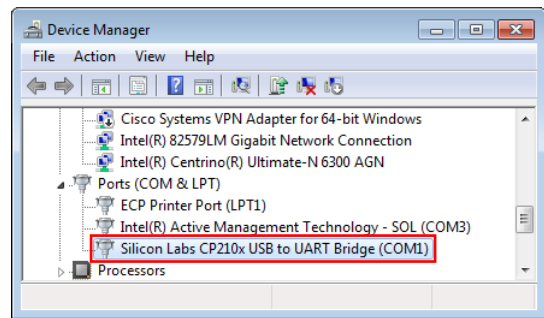


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Figure 1-1: Host Computer COM Port Configuration

2. Turn Board power on (SW12).

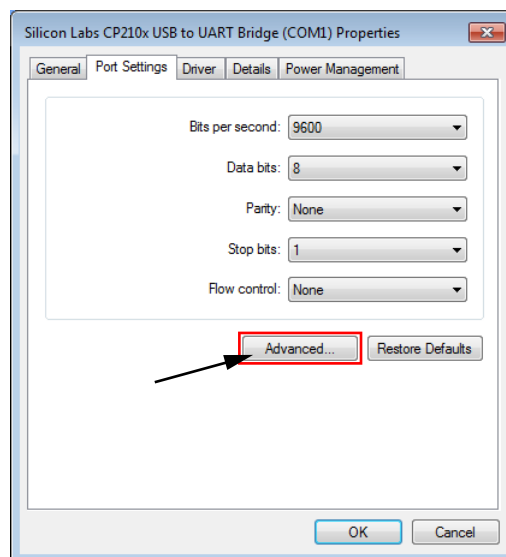
3. Open the host computer Device Manager (Figure 1-2). In the Windows task bar, Click **Start**, click **Control Panel**, and then click **Device Manager**.



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Figure 1-2: Device Manager

4. Open UART properties. Expand **Ports (COM & LPT)**, right-click **Silicon Labs CP210x USB to UART Bridge**, and then click **Properties**.
5. In the properties window, select the **Port Settings** tab, verify the settings match the values shown in Figure 1-3 and then click **Advanced**.



UG848_c1_03_071112

Figure 1-3: Port Settings

- Select an unused COM Port Number and then click **OK**. Figure 1-4 shows **COM1** as the selected COM port number.

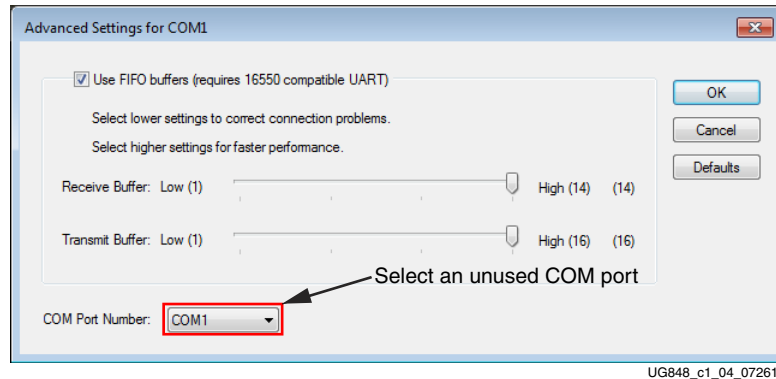


Figure 1-4: Advanced Settings

- Click **OK** in the properties window (Figure 1-3, page 7), and then close the Device Manager and the Control Panel.

Install the Terminal Program

Download and install the TeraTerm Pro terminal program on the host computer. TeraTerm Pro is available for download at no cost from <http://www.ayera.com/teraterm/>.

To communicate with the VC707 board, configure the New Connection and Serial Port settings as shown in Figure 1-5. These settings must match the host computer COM port settings shown in Figure 1-3, page 7 and Figure 1-4.

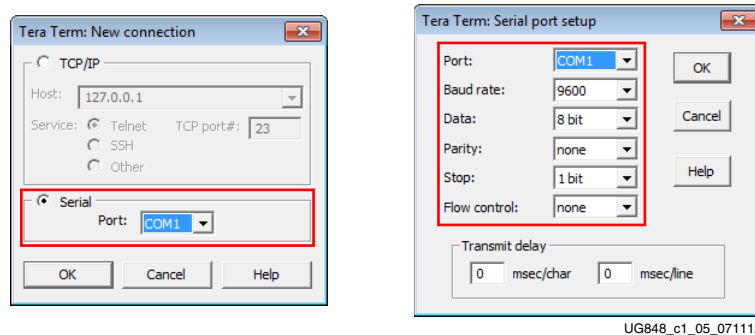


Figure 1-5: TeraTerm Pro Settings

Preliminary setup is complete and the reference designs can now be run.

Verify Jumpers are in Default Positions

Verify the jumpers on the VC707 board are positioned as shown in [Table 1-1](#).

Table 1-1: Default Jumper Positions

Jumper Connector	Function	Jumper Position
J6	SFP Enable	None
J7	EPHY Interface Mode: None = GMII/MII to copper	None
J9	XADC GND ferrite filter bypass jumper	None
J10	XADC GND-to-XADC_AGND jumper	1-2
J11	TI Controller U42 Addr 52 Reset jumper	None
J12	TI Controller U43 Addr 53 Reset jumper	None
J13	USB Mini-B Connector J2 VBUS	None
J14	USB SMBC U8 CLKOUT selector	None
J38	SFP RX Rate: 1-2 = Full BW Rate, 2-3 = Low BW Rate	1-2
J39	SFP TX Rate: 1-2 = Full BW Rate, 2-3 = Low BW Rate	1-2
J40	EPHY Interface Mode: 1-2 = GMII/MII to copper	1-2
J41	EPHY Interface Mode: 1-2 = GMII/MII to copper	1-2
J42	XADC external 1.2V or internal VREFP selector	1-2
J43	XADC VCC Select Header	2-3
J44	USB Mini-B Connector J2 GND jumper	None
J45	USB SMBC U8 VBUS	1-2
J49	PCIe® Bus Width Select Header	5-6
J50	TI Controller U64 Addr 54 Reset jumper	None
J51	FMC_VADJ_ON_B jumper	1-2
J52	FPGA U1 INIT_B-to-PROG_B jumper	None
J53	XADC VCC5V0-to-XADC_VCC5V0 jumper	1-2
J54	XADC REF3012 U35 V _{IN} Select	1-2

Built-In Self Test

The BIST tests several XC7VX485T FPGA and VC707 board features. The BIST interface is a menu of tests displayed by a terminal program running on the host computer.

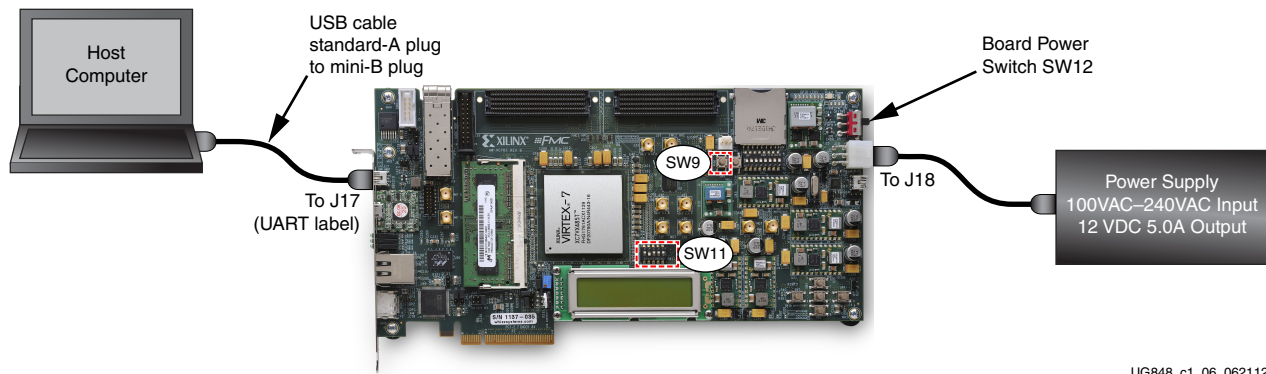
Project Files

Project files for the BIST are located in `vc707_BIST_rdf0157_<ISE revision>.zip` online as RDF0157 at: <http://www.xilinx.com/vc707>.

The BIST is pre-loaded in the device and the project files are not required to run this demonstration.

Run BIST

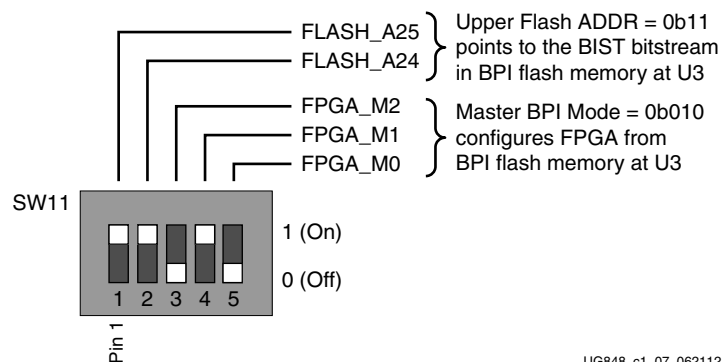
1. Complete the tasks under [Preliminary Setup, page 6](#).
2. Connect the VC707 board to the host computer and power supply as shown in [Figure 1-6](#).



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Figure 1-6: BIST Board Connections

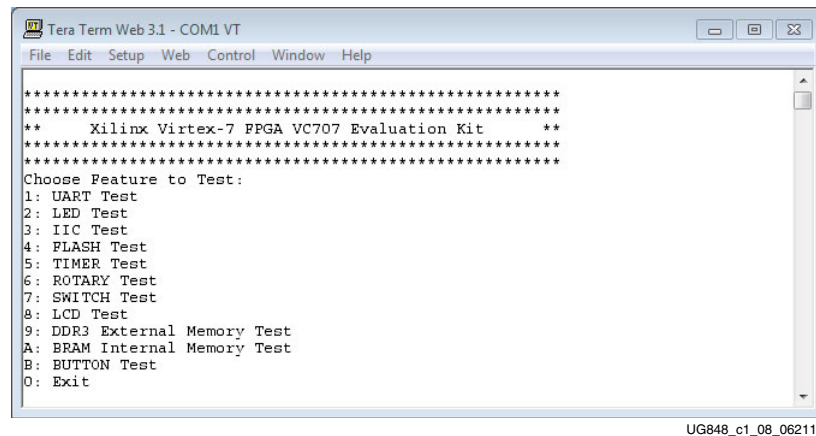
3. Turn board power on (SW12).
4. Set DIP switch SW11 as shown in [Figure 1-7](#).



UG848_c1_07_062112

Figure 1-7: SW11 BIST Settings

5. Press and release the Program button SW9 (Figure 1-6). The BIST bitstream configures the FPGA and then runs BIST. The terminal program displays the BIST menu shown in Figure 1-8.



```
Tera Term Web 3.1 - COM1 VT
File Edit Setup Web Control Window Help
*****
**      Xilinx Virtex-7 FPGA VC707 Evaluation Kit      **
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: IIC Test
4: FLASH Test
5: TIMER Test
6: ROTARY Test
7: SWITCH Test
8: LCD Test
9: DDR3 External Memory Test
A: BRAM Internal Memory Test
B: BUTTON Test
0: Exit
```

UG848_c1_08_062112

Figure 1-8: BIST Menu

6. To run a test, type the test number, and press the **Enter** key. Press any key to end the test and return to the menu.

IBERT Demonstration

The IBERT demonstration shows the operation of the GTX transceivers running in near-end PCS loopback mode using the IBERT console window provided by the ChipScope™ Pro Analyzer.

Extract the Project Files

The .cpj project and .bit files for the IBERT demonstration are located in vc707_IBERT_rdf0158_<ISE version>.zip available online at: <http://www.xilinx.com/vc707>

To extract the project files, locate the file vc707_IBERT_rdf0158_<ISE version>.zip and unzip the files to a working directory on the host computer.

Set Up the Hardware

1. Complete the tasks under [Preliminary Setup](#), page 6.

2. Connect the VC707 board to the host computer and power supply as shown in Figure 1-9.

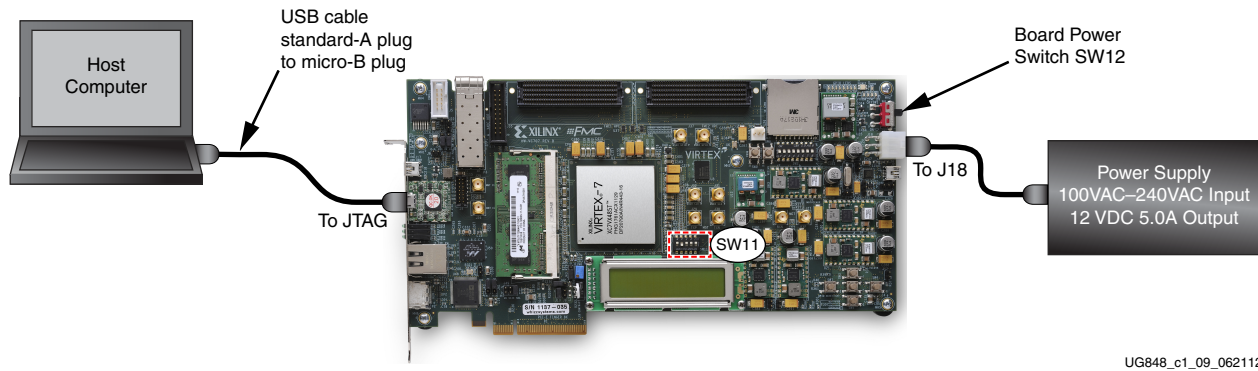


Figure 1-9: IBERT Board Connections

3. Turn board power on (SW12).
4. Set DIP switch SW11 as shown in Figure 1-10.

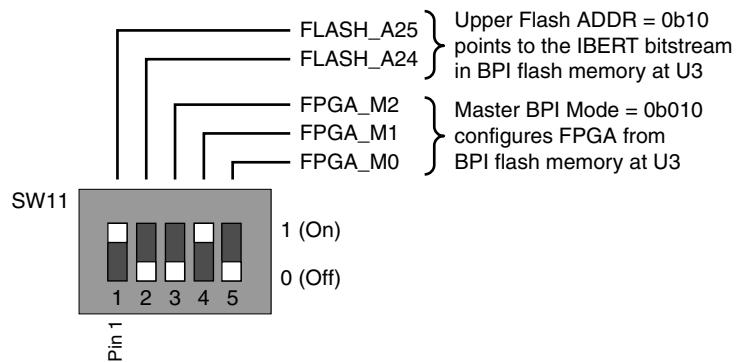
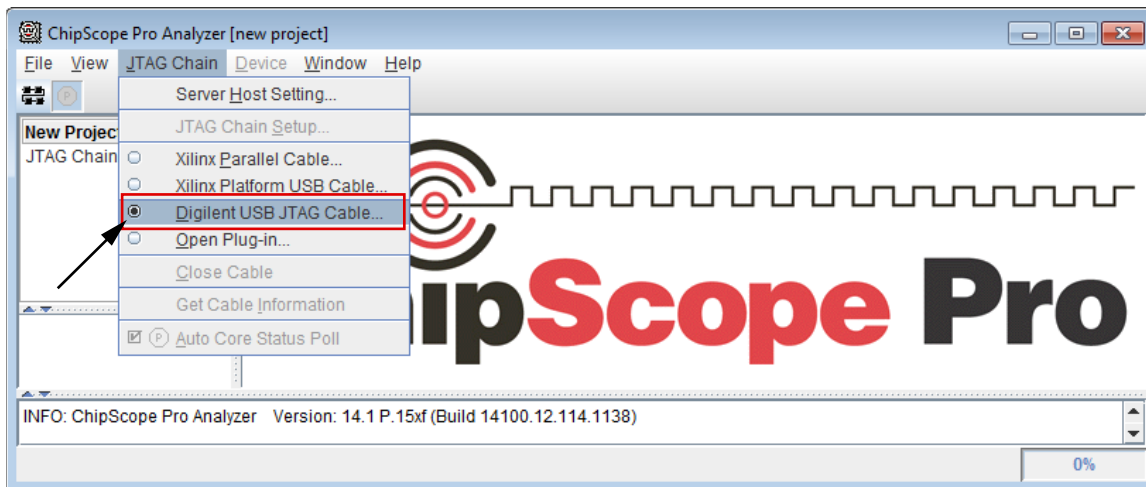


Figure 1-10: SW11 IBERT Settings

5. Press and release the Program button (SW9). The IBERT bitstream configures the FPGA and then runs the IBERT design.

Set up ChipScope Pro Analyzer

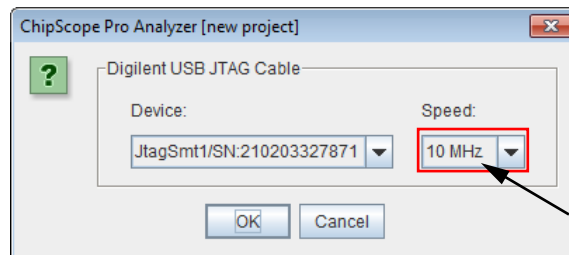
- Open the ChipScope Pro Analyzer.
Click **Start** → **All Programs** → **Xilinx Design Tools** → **ISE Design Suite XX.X** → **ChipScopePro** → ...
If the host computer system is 64-bits, open **ChipScope 64-bit** → **Analyzer**.
If the host computer system is 32-bits, open **ChipScope 32-bit** → **Analyzer**.
- Click **JTAG Chain** → **Digilent USB JTAG Cable** (Figure 1-11).



UG930_c1_11_073112

Figure 1-11: Select Digilent USB JTAG Cable

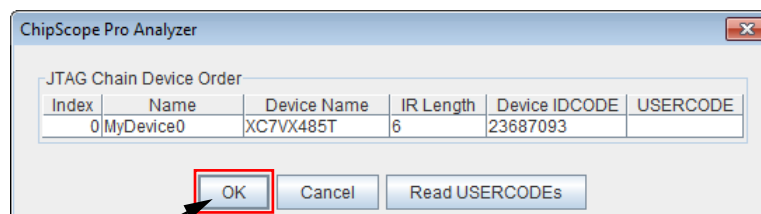
- Set the JTAG cable for 10 MHz operation and click **OK** (Figure 1-12).



UG848_c1_12_073112

Figure 1-12: Set Cable Speed

- Click **OK** (Figure 1-13).

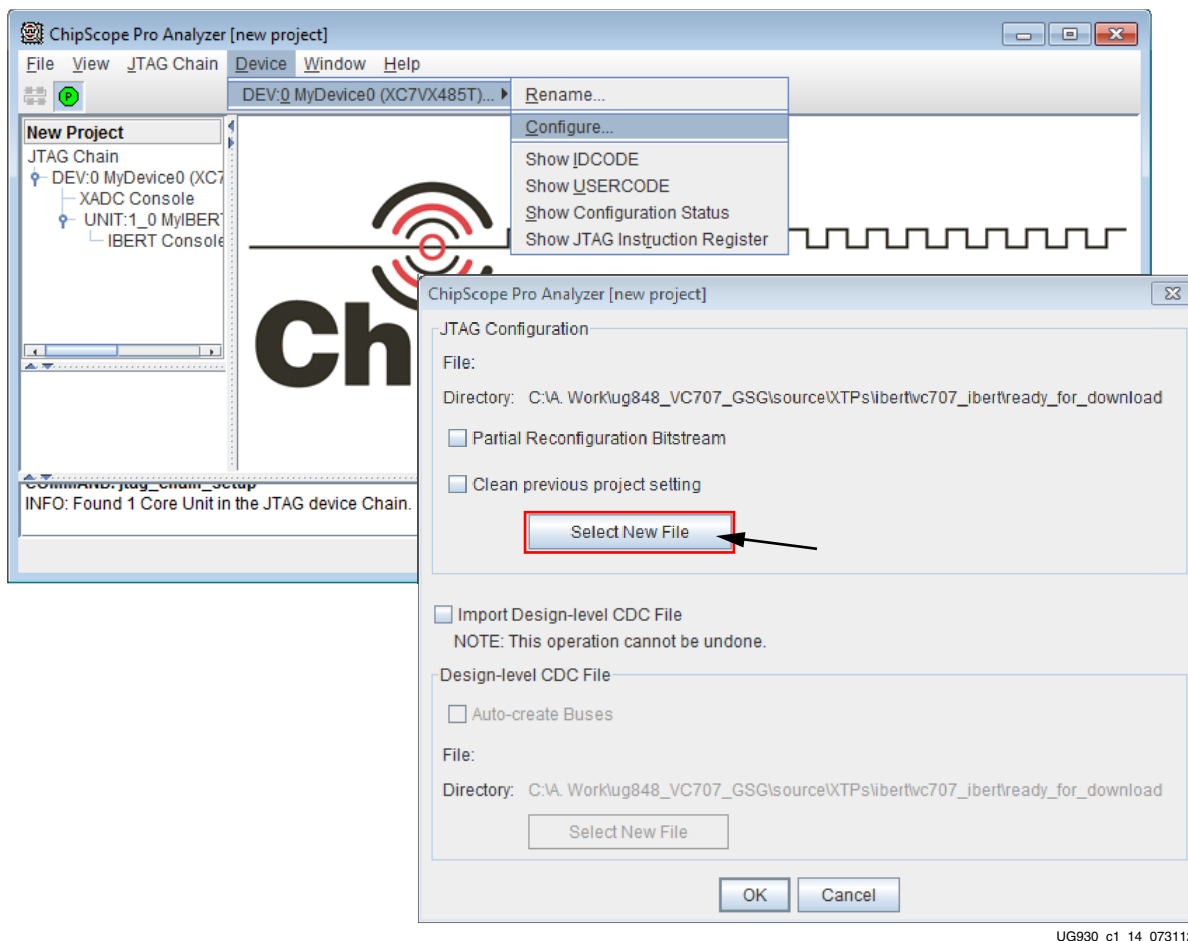


UG848_c1_13_073112

Figure 1-13: JTAG Chain Device Order

Load Bitstream File

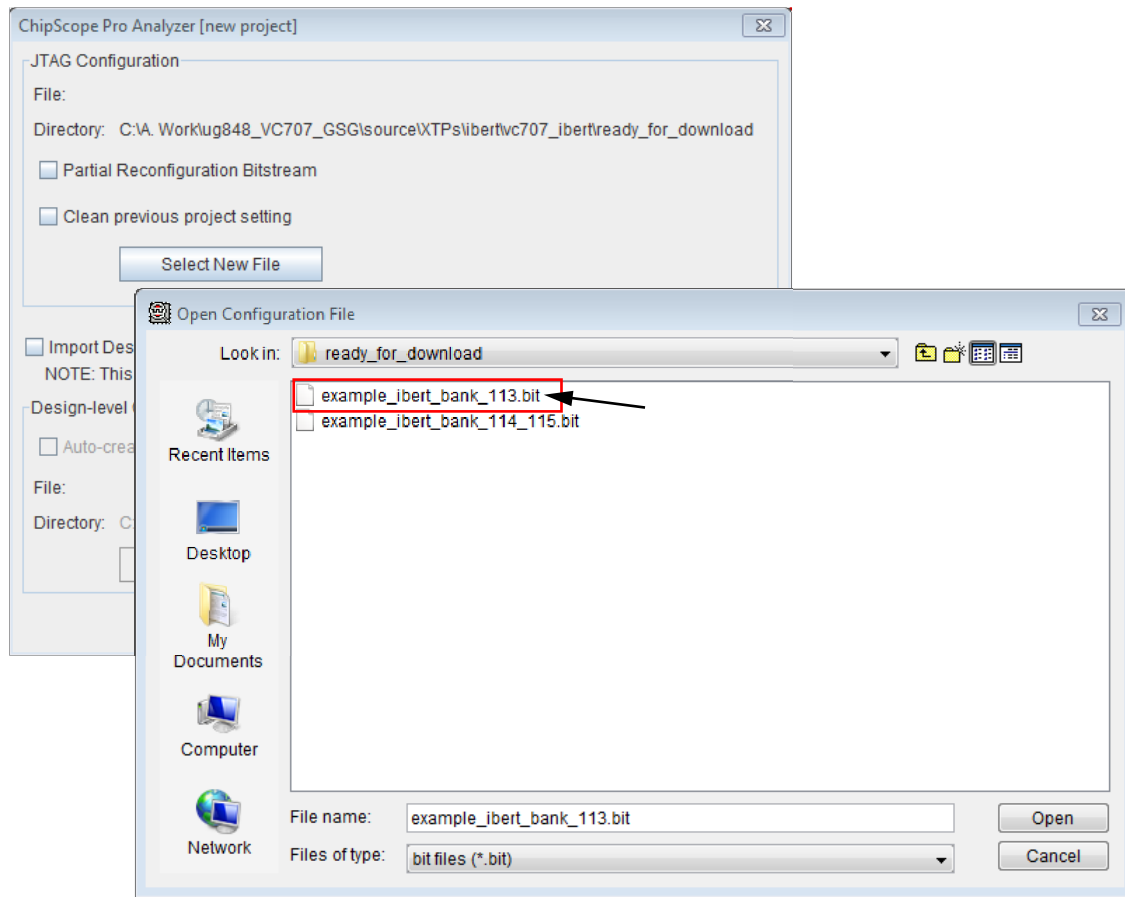
1. Click **Device** and click **DEV:0 MyDevice0 (XC7VX485T)** → **Configure** and click **Select New File** (Figure 1-14).



UG930_c1_14_073112

Figure 1-14: Select New File

2. Select `example_ibert_bank_113.bit`, click **Open**, and then click **OK** (Figure 1-15).



UG848_c1_15_073112

Figure 1-15: Select Bitstream File

Examine GTX Transceiver Operation

1. In the project panel, double-click **IBERT Console** (Figure 1-16).



UG848_c1_16_073112

Figure 1-16: Project Panel - IBERT Console (GTX)

- The status and test settings are displayed on the **MGT/IBERT Settings** tab in the IBERT Console shown in Figure 1-17. Click the BERT **Reset** button for each GTX transceiver and verify that there are no bit errors.

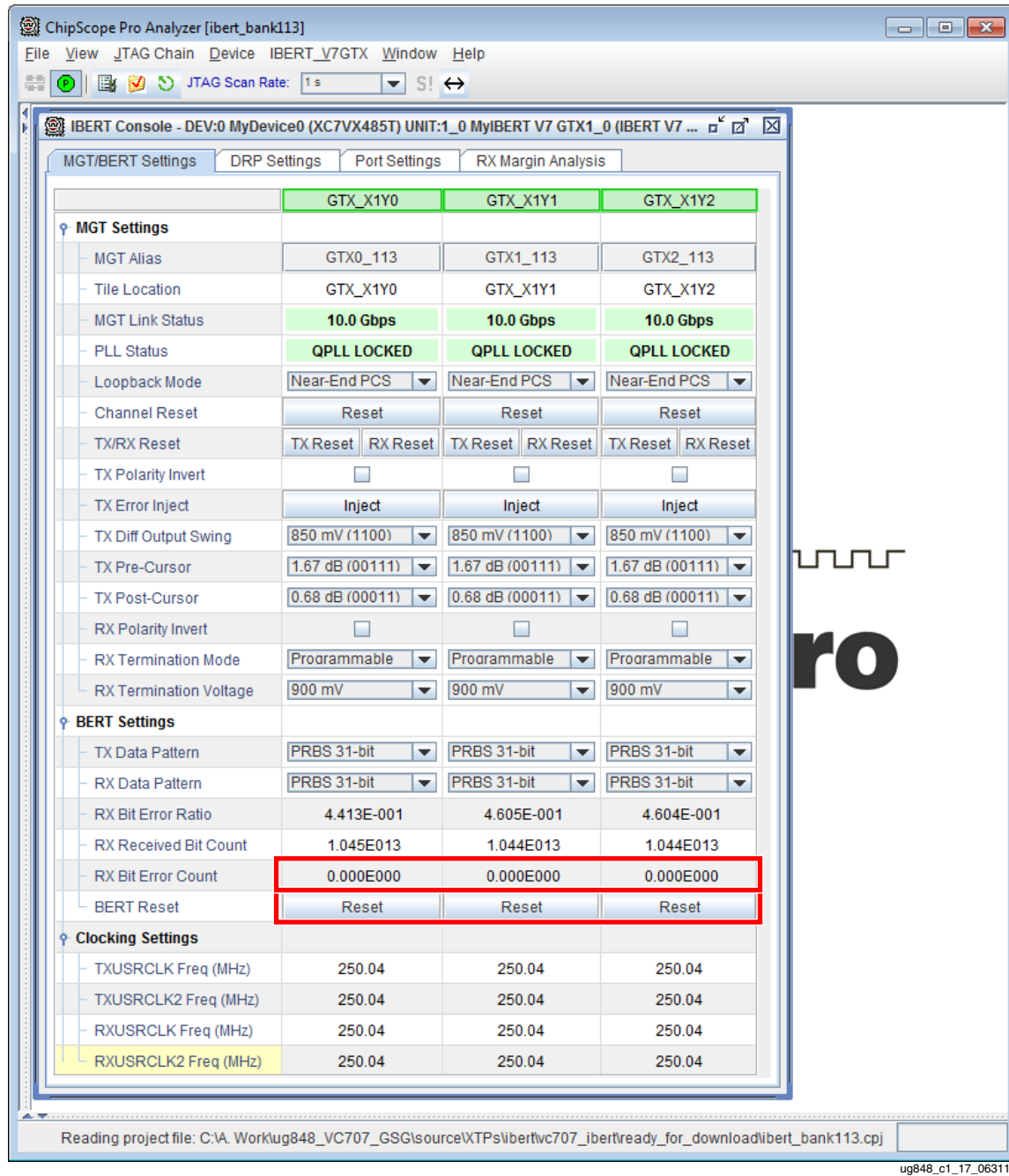


Figure 1-17: GTX IBERT Console

AMS 101 Card Demonstration

The XC7VX485T FPGA features dual one Mega-sample per second (MS/s), 12-bit, analog-to-digital converters (XADC) built into the FPGA. The AMS card demonstration uses the AMS 101 card (Figure 1-19, page 19) to generate an analog signal and the AMS evaluator tool (Figure 1-20, page 20) to view and control the signal.

Install the LabVIEW Run-time Engine

Install the National Instruments LabVIEW Run-Time Engine 2011 Installer using either [Method A](#), [Method B \(For 32-Bit Systems\)](#), or [Method C \(For 64-Bit Systems\)](#).

Method A

1. Locate the file `AMS_Eval_Demo_Files_<ISE_Version>.zip` and unzip the `AMS101_Installer.zip` folder.
2. Install the LabVIEW Run-Time Engine. Open `AMS101_Installer\Volume` and double-click `setup.exe`.
3. Reboot the host computer to complete the installation.

Method B (For 32-Bit Systems)

Download and install the National Instruments LabVIEW Run-Time Engine (32-Bit) on the host computer. The drivers are available for download at no cost from <http://joule.ni.com/nidu/cds/view/p/id/2534/lang/en> (LabVIEW 32-bit Run-Time Engine).

Method C (For 64-Bit Systems)

Download and install the National Instruments LabVIEW Run-Time Engine (64-Bit) on the host computer. The drivers are available for download at no cost from <http://joule.ni.com/nidu/cds/view/p/id/2536/lang/en> (LabVIEW 64-bit Run-Time Engine).

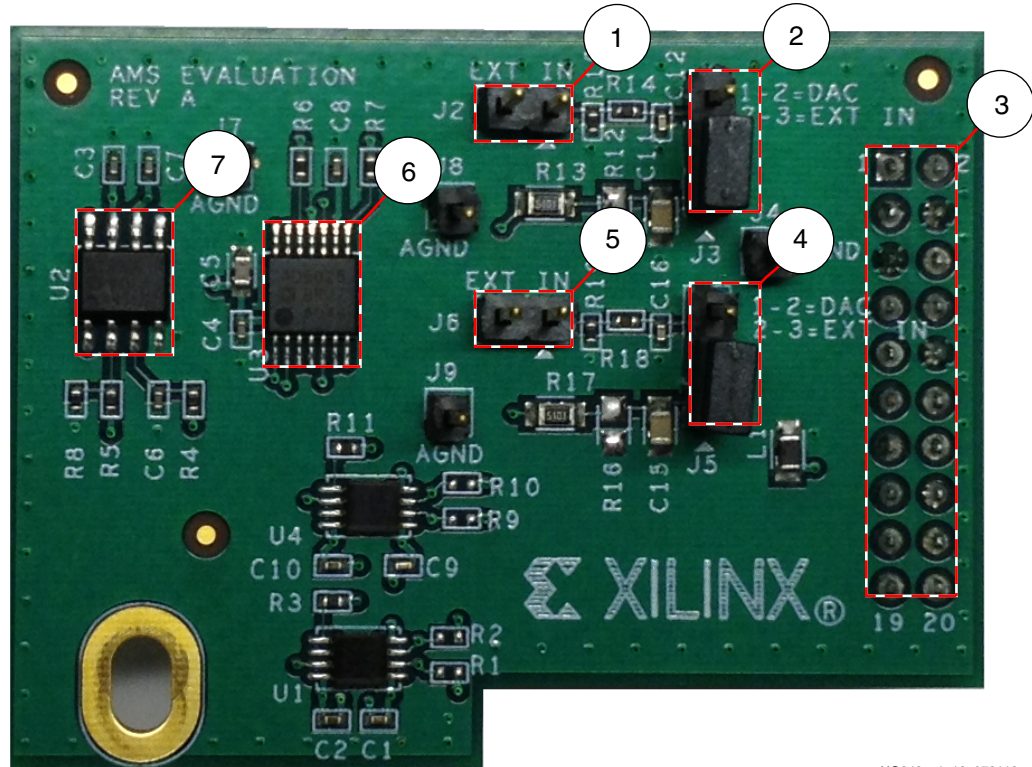
Note: The procedures for 32-bit and 64-bit host computers are identical except for the run-time engine that is downloaded.

Extract the AMS Design Files

1. Go to <http://www.xilinx.com/vc707> and navigate to the Docs & Designs tab. Download the zip file `AMS_Eval_Demo_Files_<ISE_Version>.zip`
2. Locate the file `AMS_Eval_Demo_Files_<ISE_Version>.zip` and unzip the files to a working directory on the host computer.
3. Open the ChipScope Pro Analyzer in the ISE design tools.
4. Click **Open_cable**.
5. Select **Device**, choose **Configure**, and click **Select New File**.
6. Open `AMS_VC707_Bitstream.bit` from the working directory.

Set Up the Hardware

1. Complete the tasks under [Preliminary Setup](#), page 6.
2. On the AMS101 card ([Figure 1-19](#)), place jumpers across pins 1–2 on J3 and J5.



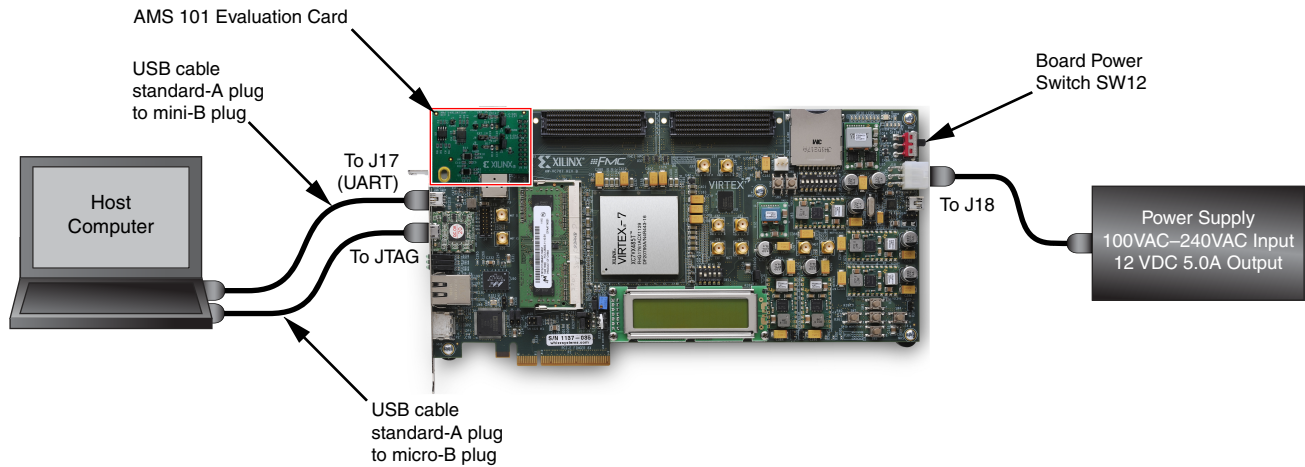
UG848_c1_18_073112

Figure 1-18: AMS101 Evaluation Card

Table 1-2: AMS101 Evaluation Card Jumper and Component Notes

Callout	Reference Designator	Notes
1	J2	External signal source input to V_P positive analog input.
2	J3	Jumper on pins 1–2 selects DAC signal source. Jumper on pins 2–3 selects external input source on J2.
3		20-pin connector to XADC header J35 on the VC707 board.
4	J5	Jumper on pins 1–2 selects DAC signal source. Jumper on pins 2–3 selects external input source on J6.
5	J6	External signal source to V_N negative analog input.
6	U3	16-bit DAC. Sets analog test voltage.
7	U2	Reference buffer for DAC.

- Plug the AMS 101 Card into the XADC header J35 on the VC707 board as shown in [Figure 1-19](#).
- Connect the VC707 board to the host computer and power supply as shown in [Figure 1-19](#).



UG848_c1_19_073112

Figure 1-19: BIST Board Connections

- Turn board power on (SW12).

Examine Analog Mixed Signal Features

The AMS evaluator tool ([Figure 1-20](#)) is useful for examining analog signals in the time and frequency domains, displaying linearity, viewing the XADC register settings, and monitoring the internal FPGA temperature sensor and supply voltages. The AMS evaluator tool also provides user-controllable decimation on the XADC output data to enhance the signal-to-noise ratio (SNR) performance.

To run the AMS evaluator tool executable file:

- Open the `AMS_Eval_Demo_Files_<ISE_Version>` directory and double-click `AMS101 Evaluator GUI V1.0.exe`. See [Figure 1-20](#).

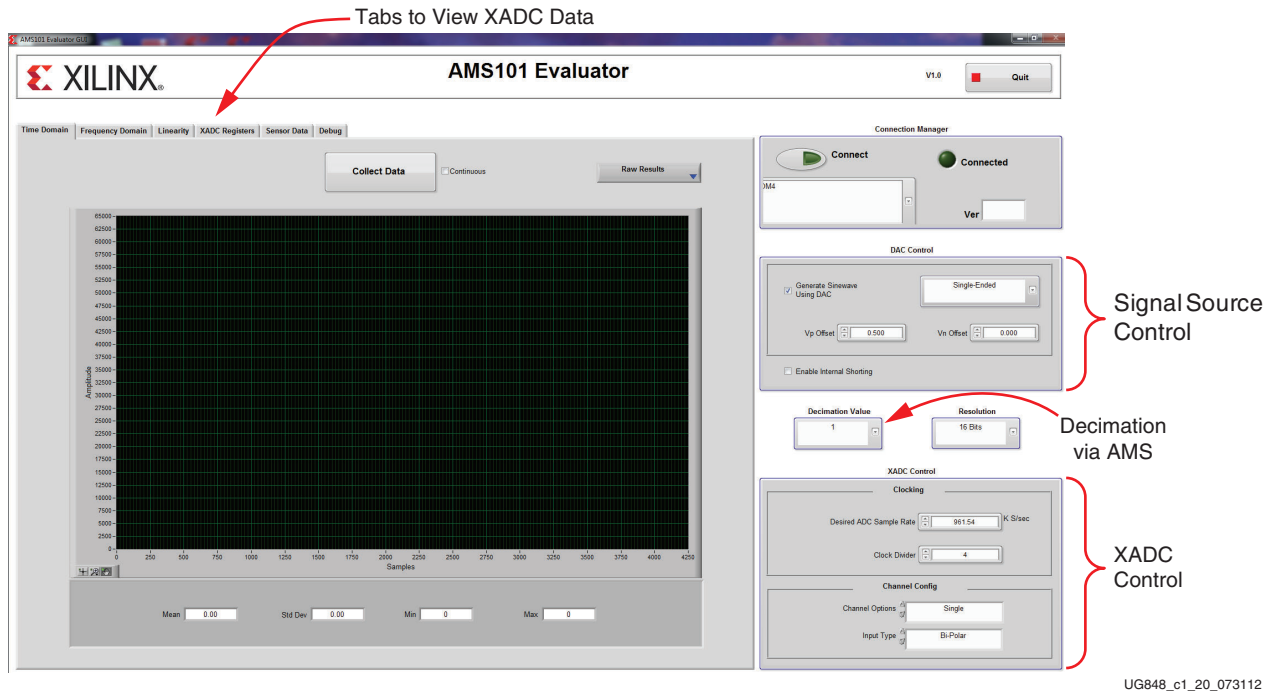


Figure 1-20: AMS101 Evaluator Tool

For an extensive explanation of the AMS101 evaluation card see [UG886](#), *AMS101 Evaluation Card User Guide*.

Multiboot Design

Files for the multiboot are located in `vc707_multiboot_rdf0159_<ISE revision>.zip` online as RDF0159 at: <http://www.xilinx.com/vc707>.

To run the multiboot reference design, set the configuration mode and flash address switch SW11 to 00001, which is Master SPI configuration from the linear flash. Connect the USB-JTAG and power cables as shown in [Figure 1-9](#), [page 12](#). Set the user switches (SW2) to 00000000. Unzip the design files to your C: drive.

1. Program the design into the SPI flash using these command line instructions:

```
cd C:\kc705_multiboot\SPI_Flash
impact -batch kc705_program_spi.cmd
```

A cycling LED pattern appears on the user LEDs.

2. Run the iMPACT tool and select options to configure the device over JTAG.

3. Read the device status and verify in the console display that only VALID_0 is set (Figure 1-21).

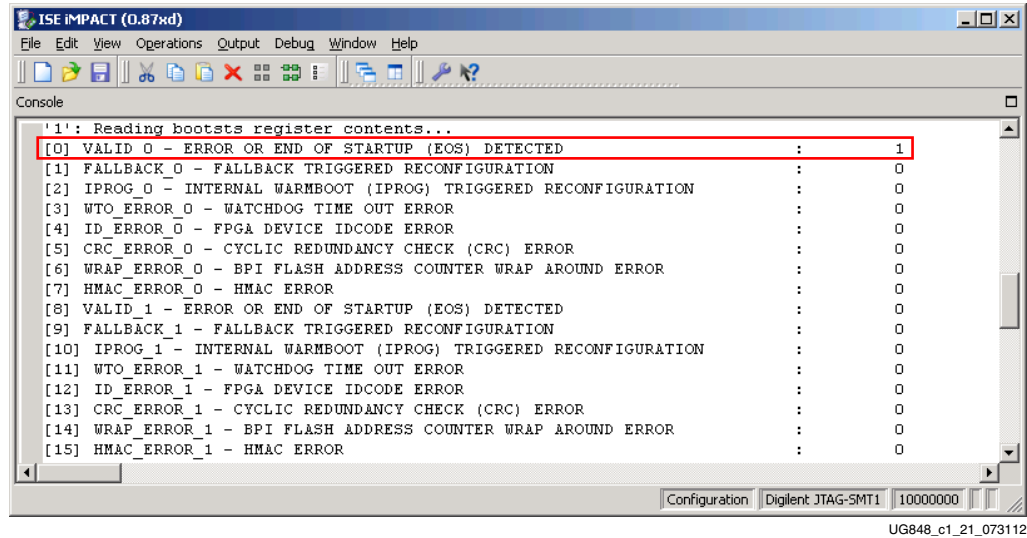


Figure 1-21: Console Display

4. Set SW2 to 10000000 to force the multiboot reboot.
5. When the DONE LED (DS10) goes out, set switch SW2 to 00000000. The LED pattern changes and the device status shows that both IPROG_0 and VALID_1 are set.
6. Press and release the Program button (SW9) to reboot back to the golden bitstream.
7. Repeat these steps, changing SW2 to 00010000 and verify that the device status IPROG_0 is no longer active, and that FALLBACK_0, IPROG_1, and CRC_ERROR_1 are active (Figure 1-22).

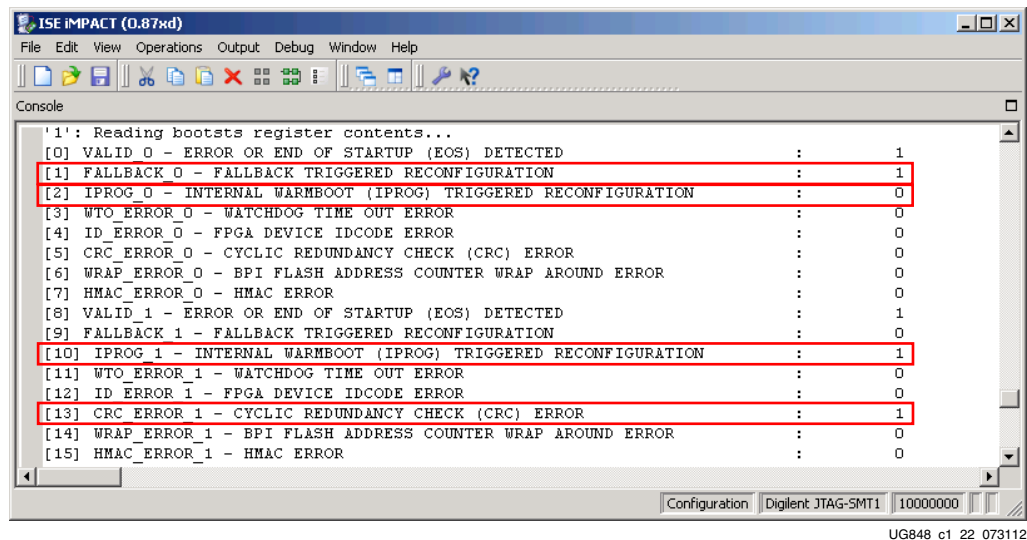


Figure 1-22: Console Display

MIG Design

Files for the MIG design are located in `vc707_MIG_rdf0160_<ISE revision>.zip` online as RDF0160 at: <http://www.xilinx.com/vc707>.

To use the MIG, first unzip the design files to your C: drive:

1. Open the ChipScope Pro Analyzer.
2. Open the cable (the top-left button) and configure the device DEV:0 MyDevice0 (XC7VX485T) with `<Design path>\mig_7series_v1_3\example_design\par\example_top.bit`.
3. After configuration, verify this LED behavior:
 - a. After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking. If LED 1 is not blinking, check the external OSC.
 - b. After about 30 seconds, LED 3 will light and stay on. Wait until LED 3 lights.
 - c. If an error occurs, LED 0 will go out and LED 2 will light.
 - d. Press SW8 to reset.
4. In ChipScope, open the project `<Design Path>\ready_for_download\vc707B_mig.cpj` and view **Waveform**.
5. Click **Trigger** to view the data waveforms and validate the design (Figure 1-23).

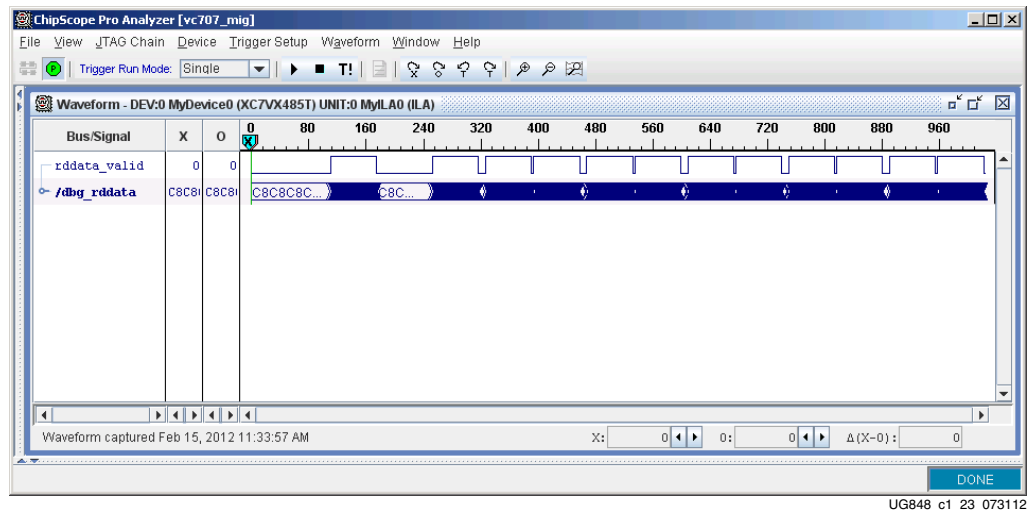


Figure 1-23: ChipScope Display

Integrated Endpoint Block for PCI Express

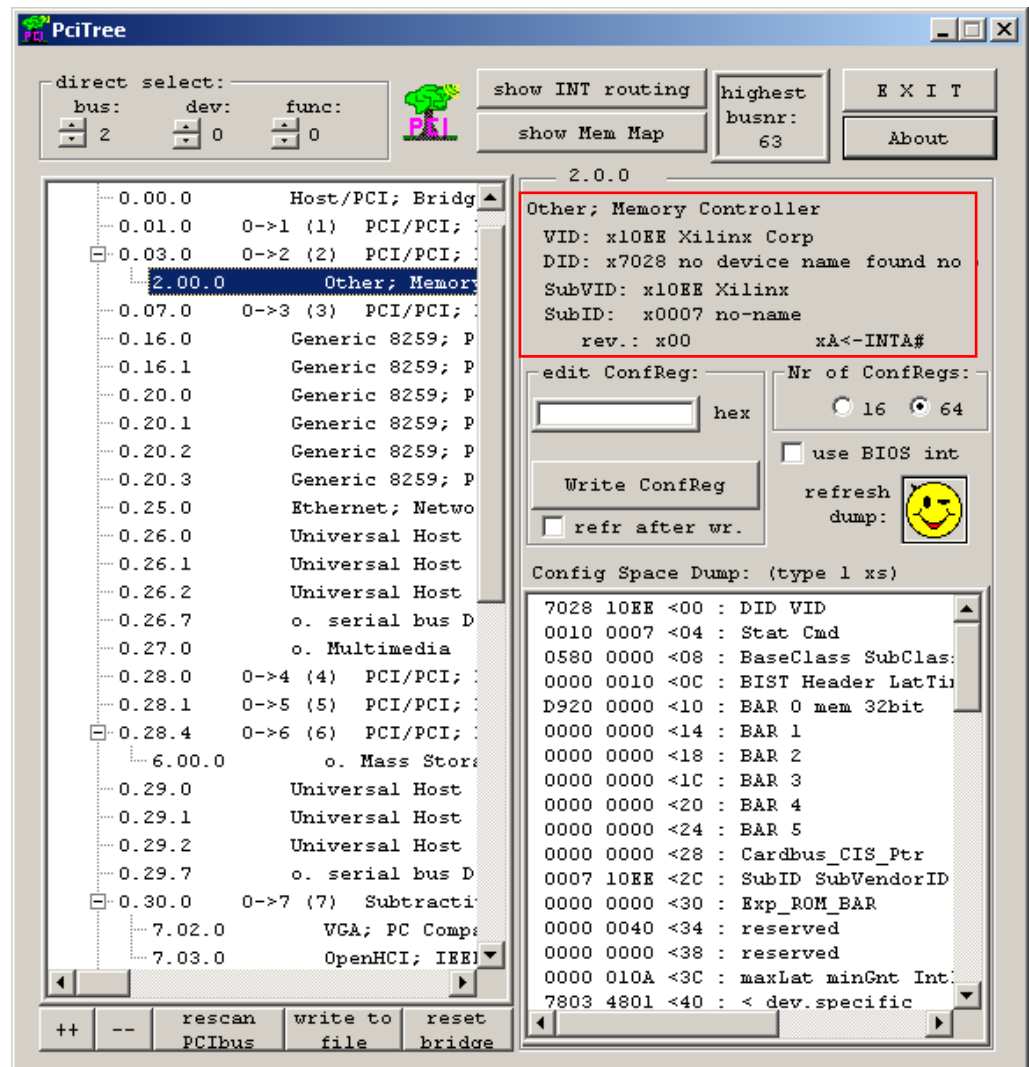
Files for this design are located in `vc707_PCIe_rdf0161_<ISE revision>.zip` online as RDF0161 at: <http://www.xilinx.com/vc707>.

To run the PCIe reference design, set up the VC707 board as described in [Preliminary Setup, page 6](#). Set the Configuration Mode and Flash address DIP switch SW11 to Master BPI mode 00010. Unzip the files to your C: drive.

Start the iMPACT tool and program the Master BPI flash with the PCIe design:

1. Perform a boundary scan and initialize the chain.

2. Add BPI flash part number 28F00AG18F, data width 16, and address bits 25:24. Right-click on FLASH to select **Program**. Choose the file:
 <design_path>\ready_for_download\kc705_pcie_x8_gen1.mcs.
3. Program with the **Erase before Programming** option.
4. Plug the VC707 board into a PCIe slot in a PC using the PC Power adapter (*not* the PCIe connector from the PC power supply).
5. Power on the PC and start up PciTree.
6. Set the number of configuration registers to 64, and Refresh Dump.
7. Locate the Xilinx device and navigate the linked list in configuration space to locate the PCIe® Capabilities Structure (Figure 1-24).



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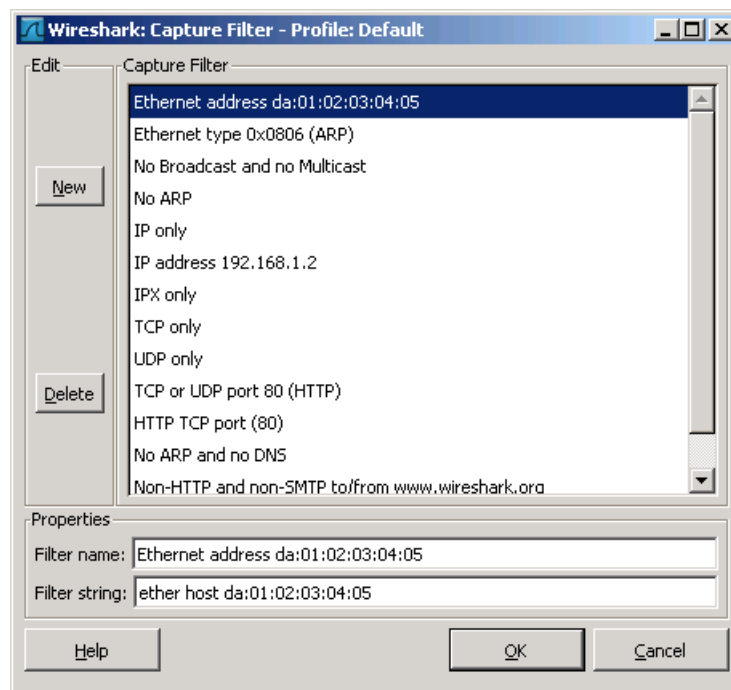
Figure 1-24: PciTree Display

LogiCORE IP Ethernet SGMII Design

Files for this design are located in `vc707_ethernet_rdf0165_<ISE revision>.zip` online as RDF0165 at: <http://www.xilinx.com/vc707>.

The Ethernet 1000BASE-X PCS/PMA or SGMII core provides the functionality to implement the 1000BASE-X PCS and PMA sublayers or can provide a GMII to SGMII/SGMII to GMII bridge when used with a device-specific transceiver. The core interfaces to a device-specific transceiver. It provides some of the PCS layer functionality, such as 8B/10B encoding/decoding, the PMA SerDes, and clock recovery.

1. Install Wireshark Protocol Analyzer version 1.6.1 (<http://www.wireshark.org/>).
2. Set up VC707 board as in [Figure 1-9, page 12](#). Add an Ethernet cable connected between the VC707 and host PC and power on the board. Unzip the design files to your C: drive.
3. Start ChipScope Pro Analyzer, and initialize the chain.
4. Configure the XC7VX485T device with `<Design Path>\ready_for_download\routed.bit`.
5. Set SW2 to 00000000. This turns off the packet generator.
6. Open Wireshark and configure the capture options as follows:
 - a. Select the PC's Gigabit Ethernet connection from the drop-down menu.
 - b. Set the capture filter as in [Figure 1-25](#).



UG848_c1_25_073112

Figure 1-25: Ethernet Core

- c. Click **Start**.
7. Set SW2 to 01000000 for a moment, then back to 00000000. This briefly turns on the packet generator.

- Check the Wireshark window for a display of the packets transmitted. [Figure 1-26](#).

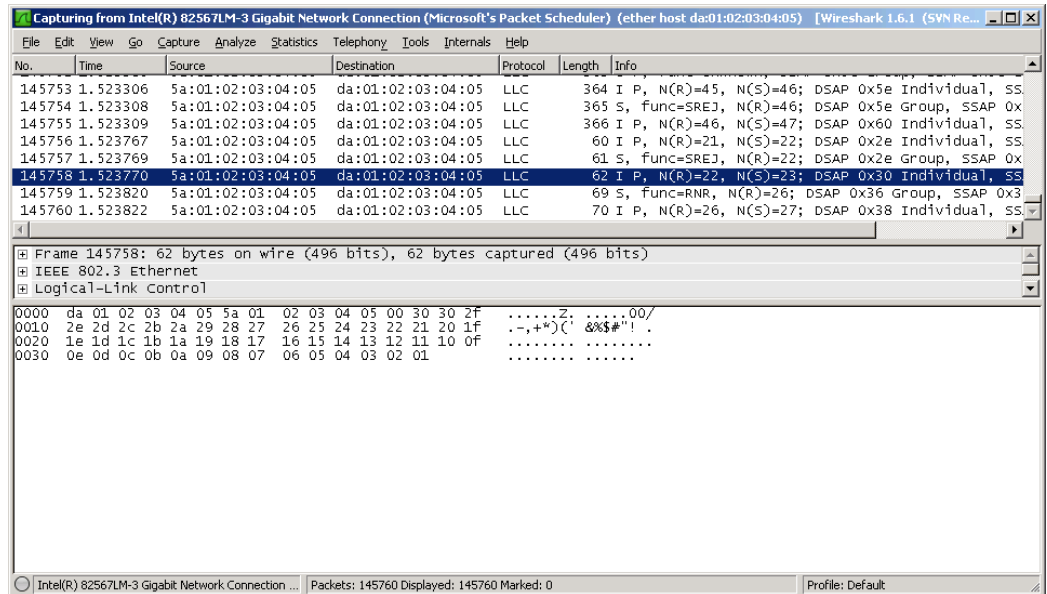


Figure 1-26: Ethernet Core

Next Steps

- Download [UG885](#), *VC707 Evaluation Board for the Virtex-7 FPGA User Guide*.
- Review and run the reference designs available at www.xilinx.com/vc707.

Additional Information

VC707 board reference design files, user guides, schematics, and bill of materials, can be downloaded from:

<http://www.xilinx.com/products/boards-and-kits/VC707>

Other documents associated with Xilinx devices, design tools, intellectual property, boards, and kits are available at the Xilinx documentation website at:

<http://www.xilinx.com/support/documentation/index.htm>

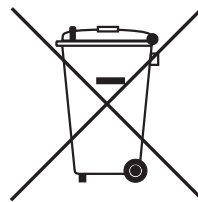
Instructions for restoring the BPI flash memory with the factory-loaded reference designs are provided in [XTP145](#), *VC707 Restoring Flash Contents*.

For an extensive explanation of the AMS101 evaluation card, see [UG886](#), *AMS101 Evaluation Card User Guide*.

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